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ORIGINAL PAPER: CHARACTERIZATION METHODS OF SOL-GEL AND HYBRID MATERIALS

# Examination on the current conduction mechanisms of Au/n-Si diodes with ZnO–PVP and ZnO/$Ag_2WO_4$ –PVP interfacial layers

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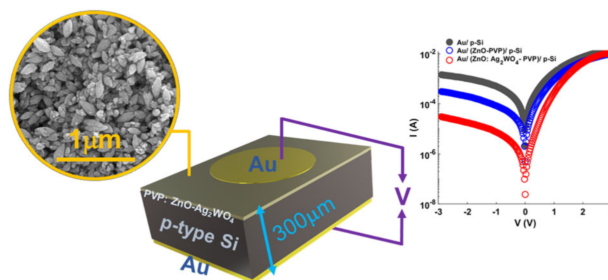
## Abstract

This study reports a comparative characterization of Au/n-Si Schottky diodes/contacts (SDs) with hydrothermally synthesized ZnO–PVP and ZnO/$Ag_2WO_4$–PVP interfacial layers, which outperforms conventional metal-semiconductor Schottky diode structures. This characterization is important because these structures outperform traditional metal-semiconductor Schottky diodes due to the presence of an interfacial layer, allowing barrier height control, surface passivation, and leakage current reduction. Based on the thermionic emission (TE) theory assumed to be the dominant current mechanism across, SDs parameters were obtained. As expected, nonlinear rectifying behavior was observed for all SDs, and the divergence from linearity is caused by factors such as the interfacial layer thickness, the interface-state ($N_{ss}$) density, and the bulk series resistance ($R_s$). It is important to note that the rectification ratio ($RR$) of the Au/(ZnO/$Ag_2WO_4$–PVP)/n-Si (MPS2) SD is 48 times more than the $RR$ of the Au/n-Si SD and 11 times greater than the $RR$ of the Au/ZnO–PVP/n-Si (MPS1) SD. The ideality factor ($n$) and zero-bias barrier height ($\Phi_{B0}$) were found to be 7.73 and 0.563 for MS, 6.23 and 0.604 for MPS, 4.83 and 0.684 for MPS2 SD. Nearly an order of magnitude less $N_{ss}$ exists for the MPS2 diode than the MS diode. According to these findings, the ZnO–PVP and ZnO/$Ag_2WO_4$–PVP interfacial layers stop Au and n-Si from reacting or diffusing with one another while also passivating the active dangling bonds at the Si surface. The methods of Cheung and Norde were also used to extract the $R_s$, $n$, and $\Phi_B$. The inconsistency between the parameters obtained from these methods could be attributed to the regions where the methods are used differ.

## Graphical Abstract

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**Keywords** ZnO–PVP and $ZnO/Ag_2WO_4$–PVP interfacial layers · Comparison of the main electrical parameters · Interface states · Cheung's and Norde's methods · Pool Frenkel Emission

**Highlights**

- ZnO–PVP and $ZnO/Ag_2WO_4$–PVP nanocomposites were hydrothermally synthesized and coated on n-Si using spin-coating method.
- The crystalline structure and morphological characteristics of $ZnO/Ag_2WO_4$ nanocomposites were studied by XRD and SEM-EDX.
- The electrical measurements show that ZnO–PVP and $ZnO/Ag_2WO_4$–PVP interfacial layers improve the fabricated diodes' interface quality and performance parameters.
- The reverse-biased conduction mechanism of the Au/n-Si (MS), Au/ZnO–PVP/n-Si (MPS1), and Au/(ZnO/$Ag_2WO_4$–PVP)/n-Si (MPS2) SDs was evaluated using Schottky or Poole-Frenkel Emission model.

## 1 Introduction

The rectifying metal-semiconductor contact, defined as the Schottky diode (SD), is based on majority carriers. Owing to their fast-switching speed, low forward voltage drop, and low junction capacitance, these diodes are widely used in optoelectronic applications [1–5]. In practice, several potential sources of error could lead to devices like SDs deviating from the ideal diode behavior and need to be considered. The quality of the metal-semiconductor SDs determines how effective integrated circuits and semiconductor devices are, and good ohmic and Schottky contacts are required for the optimal performance of these devices [6–8]. Understanding the behavior of SDs and improving their efficiency in various electronic applications necessitates an examination of their electrical properties. The following are some significant justifications for why it is crucial to examine these properties: (i) A low reverse leakage current in SDs compared to other diode types should still be analyzed to ensure that the diode meets the required specifications. High reverse leakage can cause undesirable power consumption and poor efficiency. (ii) The capacitance and frequency response of the SDs enables researchers to correctly model and simulate their behavior in various applications, assuring optimum circuit performance. (iii) Analyzing the temperature effect on the current and capacitance properties of SD is essential for applications that call for high-temperature operation or changeable environmental conditions. The charge-transport or conduction mechanisms of SD depend on several factors, including the barrier height (BH) at the M/S interface, the thickness, and homogeneity of the interfacial layer, the density-distribution of surface states/traps ($N_{ss}$), the concentration of doping atoms in the semiconductor [8–10]. The value of ideality factor ($n$) is equal to one for an ideal SD, but it is significantly greater than one ($n = 1 + d/\varepsilon_i$) ($\varepsilon_s/W_d + qN_{ss}$) due to the presence of interlayer, its thickness (d), the interlayer and semiconductor permittivity ($\varepsilon_i$, $\varepsilon_s$), the depletion layer width ($W_d$), and $N_{ss}$. Inhomogeneous barrier inhomogeneity with multiple lower barriers/patches or pinch off at approximately mean BH is also effective on conduction mechanisms. The $N_{ss}$ is typically caused by oxygen vacancies, unsaturated surface atom dangling bonds, periodic defects in semiconductor crystals, and organic contaminations in laboratory conditions. A large number of $N_{ss}$ and defects leads to a pinning of the Fermi level, resulting in the challenge of achieving high BH. The low barrier height causes high reverse leakage current and, as a result, undesirable electrical performance. Thus, controlling a Schottky barrier is important for current transmission because BH directly impact on the rectifying process. The interaction of the metal and the semiconductor is critical in this process.

The performance of SDs can be increased by reducing the flaws and dangling bonds on the semiconductor surface by depositing a thin oxide/organic interlayer among the metal and semiconductor as a passivation layer. Using an interfacial layer also reduces contact resistance and creates a barrier to prevent impurities from the metal electrode from diffusing into the semiconductor material. There have been numerous attempts to increase the performance of SDs and achieve continuous tuning of the surface states and BH at the interface of the metal/semiconductor (M/S) junction [6–10]. Çaldıran [6] fabricated the Metal/LiF/*p*-Si SDs employing various metals and Lithium fluoride (LiF) as an interfacial layer and showed that the ideal factor dropped from 1.93 to 1.48 and the BH rose from 0.69 eV to 0.78 eV when the LiF interface material was used in the device construction. Reddy et al. [7] studied the impact of the PVP polymer film interlayer on the electrical and transport characteristics of the Ti/*p*-InP MS diode. They demonstrated the increased BH from 0.76 eV to 0.87 eV, which is attributed to the PVP interlayer increasing the effective BH by altering the space charge area of InP. Thapaswani et al. [8] deposited a high-k $Ba_{0.6}Sr_{0.4}TiO_3$ (BST) interlayer on an n-InP semiconductor and showed increased rectification

ratio and barrier height for the Au/BST/n-InP SD in comparison to Au/n-InP SD. Zheng et al. [9] created the metal/n-InP by incorporating high-k dielectrics $Al_2O_3$ and $Al_2O_3$/$HfO_2$. They showed that using bilayer dielectrics decreased the effective Schottky barrier height compared to dielectric monolayer. In our previous study [10], we evaluated the influence of the PVC and $CeO_2$:PVC interlayer deposited on n-Si and reported that the leakage current ($I_0$) and ideality factor ($n$) decreased while BH increased due to the usage of PVC and ($CeO_2$: PVC) interlayers between Au and n-Si. They stated that when BH increases, the tunneling phenomena for electrons and holes is diminished and $I_0$ decreases.

The interfacial layer is chosen based on the specific application and the properties required for the device. Zinc oxide (ZnO) nanostructures have attracted much interest lately because of their unique characteristics and future uses in various industries, including electronics, optics, sensing, and biomedicine [11–14]. The following are a few of the unique qualities of ZnO nanostructures: (i) high surface area to volume ratio, which makes them perfect for catalytic and sensing applications, (ii) great mechanical strength, which provides them to be used in nanoelectromechanical systems and other mechanical applications (iii) high energy storage which provides them to be used batteries and supercapacitors (iv) a broad bandgap (3.37 eV) that allows them to work well for short-wavelength optoelectronic applications. In inorganic and polymer-based composites, the flexibility and ease of processing of organic polymers are combined with the chemical and thermal stability, high mechanical strength of inorganic materials. In general, the composite's properties are heavily influenced by the nature of its ingredients, as well as the shape, size, distribution, and crystallinity of the integrated fillers. Polyvinylpyrrolidone (PVP), a non-toxic, and environmentally friendly polymer, is commonly used as a surface capping agent for ZnO due to its film-forming properties, excellent surface passivation, and adsorption ability [12, 14]. Several researchers have examined combinations of polyvinylpyrrolidone (PVP) and ZnO for controlling optical and structural properties [11–15]. Turky et al. [12] fabricated ZnO/PVP nanocomposite fibers and reported the thermal stability and UV–Vis protection of PVP fibers were improved by adjusting the content of ZnO nanoparticles. Agulto et al. [14] evaluated the structural and optical properties of ZnO/PVP composites for possible phosphor-based applications and reported controllable and tunable emissions by varying the PVP concentration. Jambaliddini et al. [15] investigated the structural, optical, and dielectric properties of ZnO/PVP nanocomposites. They observed that the ZnO nanofillers in the PVP matrix produce wide conductive channels, improving the conducting characteristics.

Metal tungstates have been investigated for their possible use in photocatalytic and photoelectrochemical processes, batteries, capacitors, and other energy storage devices [16–18]. It has been demonstrated that the composite material silver tungstate ($Ag_2WO_4$) has numerous uses in industries like photo-catalysis, optoelectronics, and sensing [19, 20]. Several feasible interactions could take place regarding its impact on zinc oxide (ZnO). One of these interactions is the creation of a heterojunction between $Ag_2WO_4$ and ZnO, which could lead to improved photocatalytic activity by promoting charge separation and transfer. Moreover, the $Ag_2WO_4$/ZnO heterojunction can be used as a basis for new photoelectrochemical devices. Another potential effect is that the presence of $Ag_2WO_4$ on the surface of ZnO could change its electronic structure, leading to modifications in its chemical and physical properties. Several studies have been published in the literature to improve the photocatalytic and photochemical properties of $Ag_2WO_4$/ZnO heterostructures. To the best of our knowledge there are no reports about the detailed comparative study on the conduction mechanisms of ZnO–PVP and ZnO/$Ag_2WO_4$–PVP based SDs. The research paper examines the current–voltage ($I$–$V$) properties of Au/(ZnO/$Ag_2WO_4$–PVP)/n-Si (MPS2), Au/ZnO–PVP/n-Si (MPS1) and the reference Au/n-Si (MS) SBDs, where the MS interface has been altered by a thin coating of ZnO–PVP and ZnO/$Ag_2WO_4$–PVP interfacial layers. The presence of an interfacial layer improved the main electrical parameters, according to our findings.

## 2 Experimental procedures

### 2.1 Materials

In this research, the silver nitrate was used as a silver ion source, sodium hydroxide was used as a hydroxide ion source obtained from Loba Chemie, and the sodium tungstate was used as a tungsten source purchased from Merck.

### 2.2 Sample preparation

#### 2.2.1 Preparation of the ZnO sample

To prepare the ZnO sample, in the first step, 5.22 g of zinc nitrate in powder form was dissolved in 150 cc of deionized water, and then the pH value of the solution was brought to ten by adding drop-by-drop NaOH solution (5 M). The resulting solution was kept under the irradiation of ultrasound waves for 2 h. Then the resulting mixture was centrifuged and washed with water and ethanol. In the end, the resultant was dried at 60 °C for 24 h.

### 2.2.2 Preparation of the $ZnO/Ag_2WO_4$ nanocomposites

To prepare the $ZnO/Ag_2WO_4$ sample, 0.425 g of synthesized ZnO powder was dispersed in 150 cc of distilled water. Then 0.055 g of silver nitrate was mixed with the resultant and was placed under magnetic stirrer conditions for 1 h. separately, a solution of sodium tungstate (0.053 g in 50 mL of distilled water) was prepared and added drop by drop to the previously obtained solution and sonicated for 1 h. In the end, the resulting solution was washed with water and ethanol and dried at 60 °C for 24 h.

### 2.2.3 Preparation of PVP: $ZnO/Ag_2WO_4$ solution

To prepare PVP: $ZnO/Ag_2WO_4$ solution for use as the polymeric interfacial layer, 10 mg of produced $ZnO/Ag_2WO_4$ powder dispersed in 5 cc solution of PVP (5%).

### 2.2.4 The fabrication process of Au/($ZnO/Ag_2WO_4$ –PVP)/n-Si structures

$ZnO/Ag_2WO_4$–PVP suspension was prepared using a mixture of the materials in a 5% aqueous solution of PVP. The resulting suspension was then coated on the n-Si substrate utilizing the spin-coating process to create Au/($ZnO/Ag_2WO_4$–PVP)/n-Si SDs. The substrate is an n-doped single Si wafer with a (100) float zone, a thickness of~300 mm, and 1–10 Ω.cm resistivity. The standard cleaning process was used for cleaning the formed oxide layer on the surface of the n-Si substrate in the first step of washing, annealing at 55 °C and cleaning using acetone, then cleaning using distilled water and methanol and in the next step, cleaning using distilled water, solution of $H_2O$, $H_2O_2$, and $NH_4OH$ (65:13:13) at 70 °C and eventually the surface of the substrate was cleaned using a solution of HF: $H_2O$ (1:24) and washed with distilled water. In the next step, a thin (approximately 100 nm) Au layer was coated on the n-Si substrate using the sputtering method. The Au-coated substrate was annealed at 500 °C and $10^{-6}$ Torr atmosphere to achieve an excellent ohmic contact. Finally, using the spin-coating technique, the synthesized $ZnO/Ag_2WO_4$–PVP suspension was coated on the front surface of the n-Si wafer. Eventually, the Au dots with 1.2 mm diameter ($1.13 \times 10^{-2}$ $cm^2$) and ~50 nm thickness were deposited on n-Si in the same system. The electrical and dielectric properties of the fabricated Au/($ZnO/Ag_2WO_4$–PVP)/n-Si SD were characterized by Keithley (model-2400) current–voltage source meter and KEYSIGHT impedance analyzer (E4980Al 20 Hz–1MHz) at room temperature, respectively.

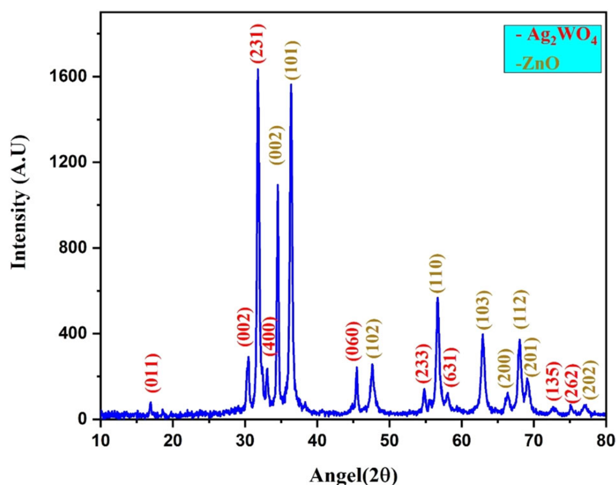



Fig. 1 XRD pattern of as-prepared $ZnO/Ag_2WO_4$ nanocomposites

## 3 Results and discussion

### 3.1 Structural and morphological characterizations

#### 3.1.1 XRD

Figure 1 shows the X-ray diffraction pattern of the $ZnO/Ag_2WO_4$ nanocomposites. In this pattern, the peaks appearing at position $2\theta = 34.5°$, 36.4°, 47.6°, 56.7°, 62.9°, 66.4°, 68.1°, 69.1° and 77.1° related to (002), (101), (102), (110), (103), (200), (112), (201) and (202) crystal planes, respectively, that correspond to the ZnO sample with wurtzite structure (PDF code no: 01-080-0075).

The rest of the peaks at $2\theta = 16.9°$, 30.5°, 31.8°, 33.0°, 45.5°, 54.8°, 58.1°, 72.7°, and 75.2° are reflected from (011), (002), (231), (400), (060), (233), (631), (135) and (262) crystal planes, respectively, which correspond to the tetragonal $Ag_2WO_4$ (PDF code no: 00-034-00615). The obtained results fully agree with the previously published reports [21, 22].

Debye-Scherrer equation was utilized to calculate the mean nanocrystallite size of the prepared nanostructures [22]:

$$D = \frac{k\lambda}{\beta \cos(\theta)} \quad (1)$$

In this equation, $k$ is constant number ~0.94, $\lambda$ is the X-ray wavelength (~1.5406 Å), $\beta$ is the full width at half maximum (FWHM) of the peak, and $\theta$ is the Bragg angle. Each component of the $ZnO/Ag_2WO_4$ nanocomposite has a different contribution to the size of the nanocrystallites, which can be calculated by using the FWHM of the peaks and with the help of Scherer's equation. The average nanocrystallite size the related to ZnO and $Ag_2WO_4$ is almost 36 nm and 32 nm, respectively.

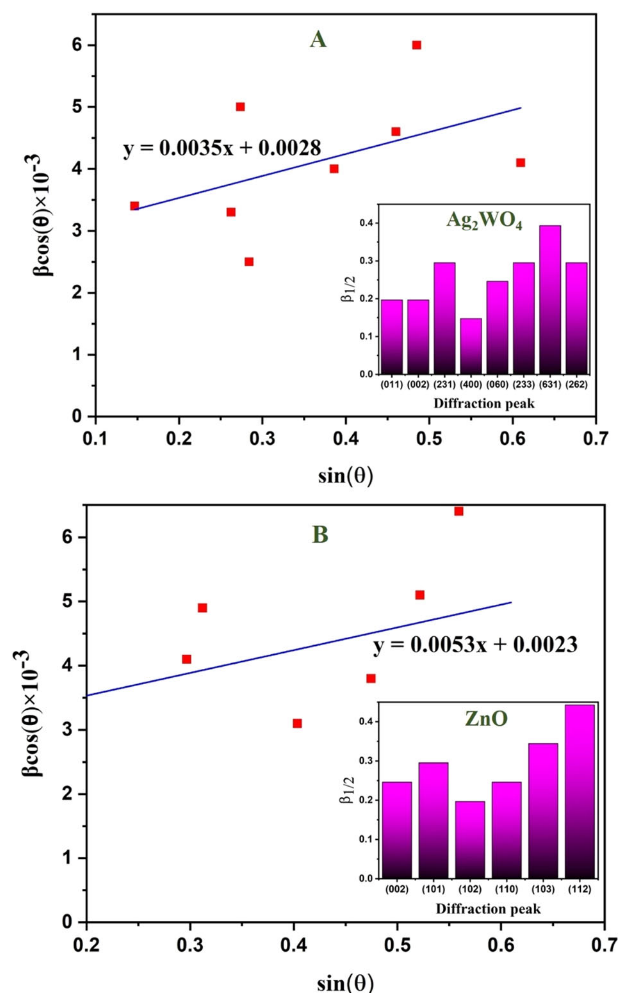



**Fig. 2** Williamson–Hall Plot and Histogram of $\beta_{1/2}$ with different diffraction peaks of **A** $Ag_2WO_4$ and **B** ZnO

It is well-known that the structural characteristics of the samples are influenced by lattice imperfections because of lattice displacements, impurities, and lattice dislocations. This investigation highlights that the impact of the abovementioned factors results in stress induction within the nanocrystalline lattice. Consequently, this leads to a significant widening and intensification of the Bragg peaks and alongside potential shifts. It is pertinent to note that the Williamson–Hall method is a widely recognized approach that can elucidate this phenomenon's underlying physics. By utilizing this method, it is possible to quantitively determine both the mean size of the nanocrystallites and the degree of strain attributed to crystal lattice stress. The following equation represents the mathematical expression of the Williamson–Hall method [23]

$$\beta\cos(\theta) = \varepsilon \times \sin(\theta) + \frac{k\lambda}{D} \tag{2}$$

In this equation, $\varepsilon$ is the strain amount. The rest of the factors are like the Debye-Scherrer equation. Additionally, Fig. 2(A, B) displays the Williamson–Hall Plot and histogram of full width at half maxima plot($\beta_{1/2}$) about distinct diffraction peaks of both constituents of the ZnO/$Ag_2WO_4$ nanocomposite, which was used in the calculation of the crystallites size. According to the Williamson-Hall equation and analyzing the slop of the linear plot of $\beta\cos(\theta)$ with respect to $\sin(\theta)$, we derived an estimate for the average crystallite size as well as the strain value of $Ag_2WO_4$ and ZnO. Specifically, the obtained values are approximately equal to 50 nm, $3.5\times10^{-3}$, and 60 nm, $5.3\times10^{-3}$, respectively.

### 3.1.2 SEM and EDX

SEM images have been used to study the morphology of the synthesized materials. Figure 3 shows SEM images of ZnO/$Ag_2WO_4$ nanocomposites in two scales. The nanocomposites contain spherical nanoparticles that were formed leaf-like nanoclusters with length of about 200 nm and width of approximately 500 nm.

Elemental analysis of ZnO/$Ag_2WO_4$ nanocomposites was done by profile EDX. Figure 4 shows the weight percent of elements prepared nanocomposites. It can also be seen from Fig. 4, this profile shows only O, Zn, Ag and W elements without additional impurities and is in agreement with the XRD results.

## 3.2 Electrical characteristics

Figure 5 depicts comparative semi-logarithmic plots of Au/n-Si (MS), Au/ZnO–PVP/n-S (MPS1) and Au/(ZnO/$Ag_2WO_4$–PVP)/n-Si (MPS2) SDs. According to Fig. 5, the presence of ZnO–PVP and ZnO/$Ag_2WO_4$– PVP interfacial layer between the Au/n-Si interface resulted in a lower reverse current and an exponential increase in forward current, indicating superior rectification properties of the MPS SD. the diode's calculated rectifying rate ($RR = I_F/I_R$) increased from 6.9 to 332.5 with the interfacial layer. It is worth noting that the $RR$ of the $MPS_2$ SD is 48 times greater than that of MS and 11 times greater than that of $MPS_1$.

The quality of the interfacial layer can have a considerable impact on the rectification behavior. By carefully selecting and adjusting the thickness and doping rate of the interfacial layer, it is possible to control the barrier height and improve $RR$. The lower $RR$ of SDs is typically caused by the presence of high series resistance, surface states, a conventional insulator layer with a lower dielectric value, barrier inhomogeneity, non-uniform interface, and highly doped donor/acceptor atoms in the semiconductor, etc. Some researchers have attempted to improve $RR$ and SD performance by adopting alternative interlayers. Çetinkaya

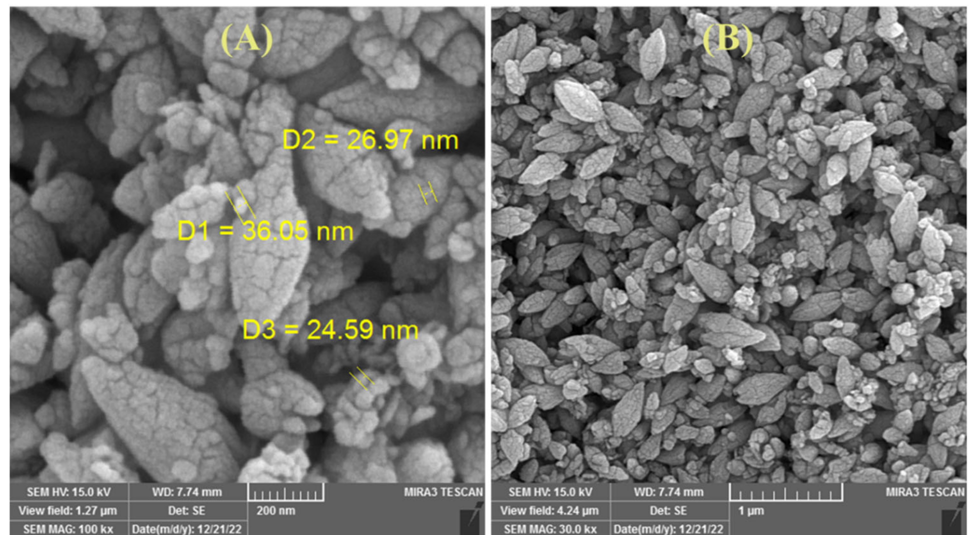
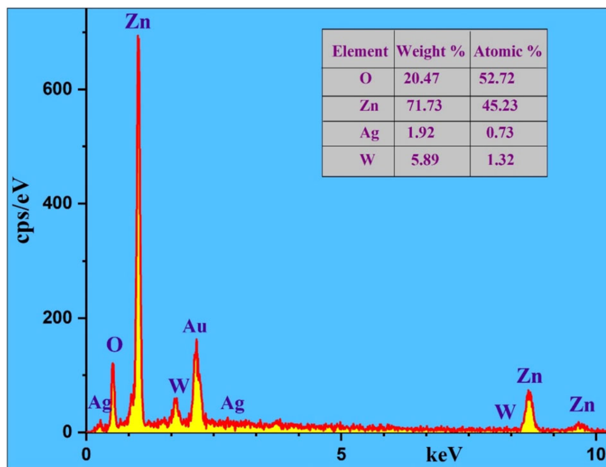



**Fig. 3** SEM images of the ZnO/$Ag_2WO_4$ nanocomposites in; **A** 100 kx and **B** 30 kx scale




| Element | Weight % | Atomic % |
|---|---|---|
| O | 20.47 | 52.72 |
| Zn | 71.73 | 45.23 |
| Ag | 1.92 | 0.73 |
| W | 5.89 | 1.32 |

**Fig. 4** EDX profile of the ZnO/$Ag_2WO_4$ nanocomposites

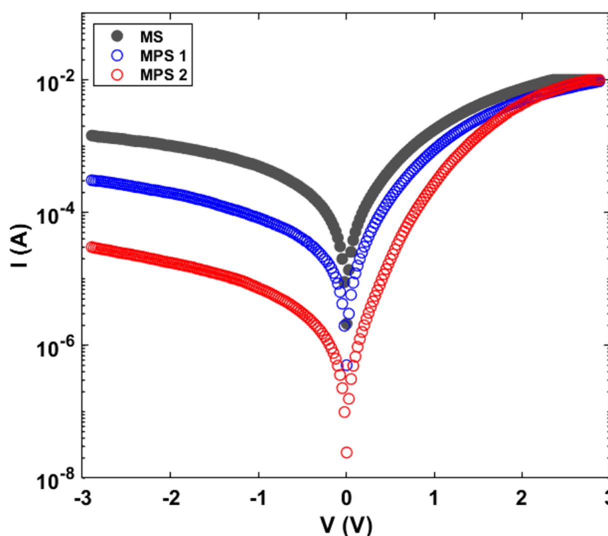



**Fig. 5** The semi-logarithmic and *I–V* curves for MS, MPS1 and MPS2 SDs

et al. [24] investigated the *I–V* properties of Au/n-Si SDs with Graphene (GP)–$Ca_{1.9}Pr_{0.1}Co_4O_x$ doped poly(vinyl alcohol) interfacial layer with different GP rates. They reported that the optimal GP doping rate for high *RR* is %7. Rodriguez et al. [25] studied the effect of Al doping on CdS thin film-based SD and discovered that when the Al doping rate increases, the ideality factor falls while the *RR* increases. Consequently, it is crucial to thoroughly understand device's properties, to optimize carefully, and to characterize the device experimentally. The type of interfacial layer, its thickness, doping material, and rate are necessary in the design and optimization process to achieve the desired rectification properties.

The *I–V* plots showed a slight deviation from linearity at higher forward voltages due to the effect of series resistance. The conventional thermionic emission theory has been used to study the current conduction mechanism of the fabricated MS, MPS1 and MPS2 SDs, and the *I–V* relation of the SD type structures with series resistance ($R_s$) can be expressed as follows [26–29]:

$$I = AA^{*}T^{2}\exp\left(-\frac{q\phi_{B0}}{K_{B}T}\right)\left[\exp\left(\frac{q(V-R_{s})}{nK_{B}T}-1\right)\right] \quad (3)$$

where $V$, $q$, $n$,$K_B$,$T$ and $\Phi_{Bo}$ are defined as the applied bias voltage, the electronic charge, the ideality factor, the Boltzmann constant, the absolute temperature and the zero-bias barrier height. The reverse saturation current ($I_o$) can be written as follows:

$$I_{0} = AA^{*}T^{2}\exp\left(-\frac{q\phi_{B0}}{K_{B}T}\right) \quad (4)$$

The $I_o$ of the diodes calculated from the intercept of the linear region of ln(*I*)–*V* plots (Fig. 6) is varied from

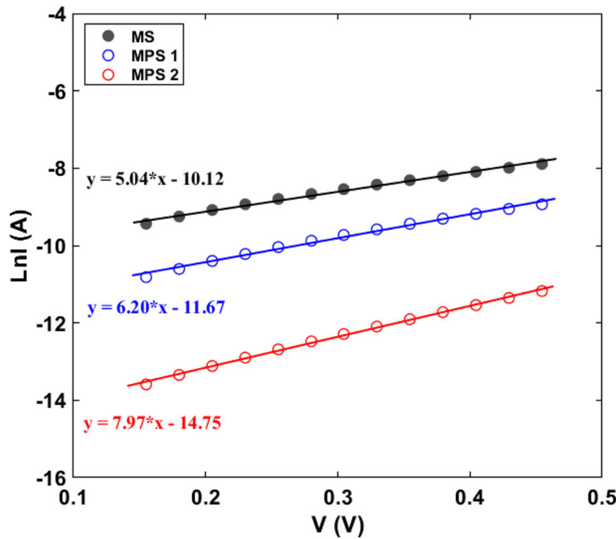



**Fig. 6** The plots of Ln$I$–$V$ for MS, MPS1, and MPS2 SDs

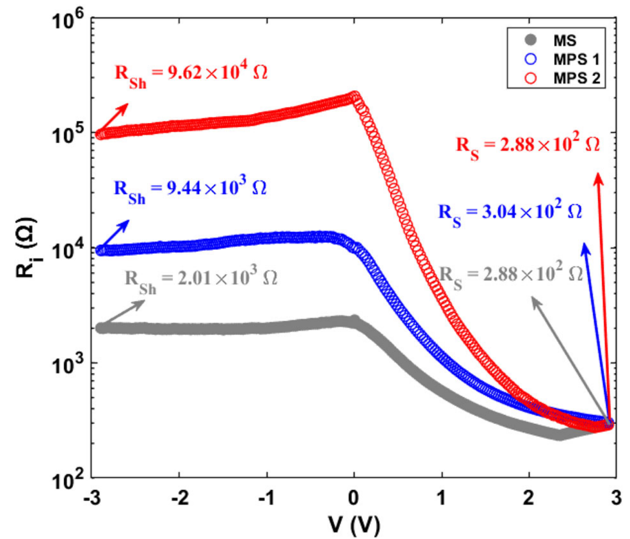



**Fig. 7** The semi-logarithmic $R_i$-$V_i$ plots of MS, MPS1, and MPS2 SDs

**Table 1** Main electrical parameters calculated from the conventional $I$–$V$ method for MS, MPS1 and MPS2 SDs

| | MS | MPS1 | MPS2 |
|---|---|---|---|
| Slope | 5.04 | 6.20 | 7.97 |
| Int. Point | −10.12 | −11.62 | −14.75 |
| $I_o$ (A) | $4.03 \times 10^{-5}$ | $8.29 \times 10^{-6}$ | $3.73 \times 10^{-7}$ |
| $n$ | 7.73 | 6.23 | 4.83 |
| $\Phi_{Bo}$ (eV) | 0.563 | 0.604 | 0.684 |
| $R_s$ (Ω) | 287.75 | 304.08 | 287.75 |
| $R_{sh}$ (Ω) | 2009 | 9441 | 96,171 |
| $RR$ | 6.9 | 30.9 | 332.5 |

$4.03 \times 10^{-5}$ to $3.73 \times 10^{-7}$, as shown in Table 1. The ideality factor ($n$) and $\Phi_{Bo}$ of all the structures were calculated from Eqs. 5 to 6, respectively. The MS SD's estimated n value is 7.72, which is discovered to be dropped to 6.23 and 4.83 when ZnO–PVP and ZnO/$Ag_2WO_4$–PVP layers are sandwiched between the Au/n-Si junction. It should be noted that all of the $n$ values greater than one can be attributed to the inhomogeneity of a thin interfacial layer and, as a result, the bias voltage dependency of the $\Phi_B$ [19, 20]. The $n$ values of the MPS1 and MPS2 structures are lower than that of the MS-type SD, owing to the passivation effect of ZnO–PVP and ZnO/$Ag_2WO_4$–PVP interlayer. [30, 31]. On the other hand, the $\Phi_{Bo}$ values for MS, MPS1 and MPS2 SDs are found to be 0.56, 0.60, and 0.68 eV, respectively. This increase may be attributed to the reduction of electron tunneling at (ZnO/$Ag_2WO_4$–PVP)/n-Si junction [31]. The decrease in the electron tunneling effect between ZnO–PVP and n-Si as well as between ZnO/$Ag_2WO_4$–PVP and n-Si interface, may be the cause of the increase in $\Phi_{Bo}$ following the addition of an interfacial layer. Furthermore, changes in semiconductor band bending caused by interactions between the metal layer and the substrate can be another reason of $\Phi_{Bo}$ alterations [32].

$$n = \frac{q}{K_B T}\left(\frac{d(V)}{d(\ln(I))}\right) \tag{5}$$

$$\Phi_{Bo} = \frac{K_B T}{q} \ \mathrm{In}\left(\frac{AA^* T^2}{I_0}\right) \tag{6}$$

The performance characteristics of a SD, such as its forward voltage drop, switching speed, and reverse leakage current, are significantly influenced by the $R_s$ and shunt resistance ($R_{sh}$). Hence, these resistances are crucial in determining the overall performance of the diode. The $R_i$ vs. $V_i$ plots depicted in Fig. 7, were used to compute the $R_{sh}$ and $R_s$ values of the diodes using Ohm's Law. The $R_i$ of the MS, MPS1 and MPS2 SDs displayed nearly constant values in reverse bias and were discovered to decrease toward forward voltage steadily. The $R_{sh}$ values of the diodes were found to be improved from 9441 Ω to 96,171 Ω (at −2.9 V). Compared to the MS diode, the MPS1 and MPS2 achieved good $R_{sh}$ values of about $10^4$ and $10^5$ Ω, respectively, closer to the ideal SD. The calculated $R_s$ values are 287.74, 304.08 and 287.74 Ω (at 2.9) for MS, MPS1 and MPS2, respectively. We demonstrated that the $R_s$ and $R_{sh}$ are extremely sensitive to the applied voltage and interfacial layer.

According to the literature, the thermionic emission (TE) theory is applied for $V \geq 3kT/q$, which corresponds to 0.075 eV at 300 K, where the conduction across the metal-semiconductor junction is principally driven by the thermionic emission process, in which electrons in the metal gain enough energy to surpass the energy barrier and enter

the semiconductor [33–35]. The main electrical parameters estimated from thermionic emission (TE) theory in Schottky diodes are approximations based on specific assumptions. The $R_s$ and $N_{ss}$ are assumed to be zero in pure TE theory, and the ideality factor is assumed to be one. In practice, however, the situation is rather different. Because regardless of how carefully the diode is prepared, neither the $R_s$ nor the $N_{ss}$ values can be zero, and the $n$ value will be significantly greater than one. While TE theory provides useful approximations for calculating these electrical parameters, the actual behavior of Schottky diodes can deviate from theory due to additional conduction mechanisms originating from interface states, surface effects, tunneling, temperature dependence, and material properties. As a result, different techniques that account for these deviations and anomalies are frequently used for proper evaluation of the electrical characteristics of actual Schottky diodes.

Compared to MS and MIS type SDs, MPS type SDs have several advantages since an interlayer of inorganic and polymer-based composite material at the M/S interface can inhibit interface diffusion and reactivity and deactivates various surface states. When BH is composed of several patches or lower BHs, charge carriers with insufficient energy to get over the mean or high barrier can easily pass through these lower barriers or patches, resulting in a rise in the current or ideality factor. In other words, barrier inhomogeneity causes an extra current to flow due to these patches or lower barriers around the mean value of BH, resulting in a larger ideality factor, as illustrated in Table 1.

The thermionic emission theory satisfactorily explains the transport characteristics of diodes at low bias values, but it cannot describe the behavior of diodes at higher voltages. It is primarily caused by the fact that in the theory of thermionic emission, the influence of $R_s$ has been disregarded as it becomes more pronounced at higher bias voltages. When the current is high, there is a deviation from the ideality, which is affected by several parameters, such as the thickness of the interfacial layer, the $N_{ss}$ at the interface, and the bulk $R_s$. The $R_s$ can be determined through Cheung's method [36], which also serves as another method to evaluate the FB using the following equations:

$$\frac{dV}{d(\ln I)} = n\left(\frac{K_B T}{q}\right) + IR_s \tag{8a}$$

$$H(I) = n\Phi_{Bo} + IR_s \tag{8b}$$

From the intercept and the slope of $dV/d\ln(I)$–$I$ plots, the $n$ and $R_s$ values of MPS1 and MPS2 structures using Eq. 8(a) are shown in Table 2. These parameters are different from those obtained from $I$–$V$ plots. The thermionic emission theory, as shown above, satisfactorily explains the transport characteristics of diodes at low bias values, but it is unable to describe the behavior of diodes at higher voltages. This is primarily caused by the fact that in the theory of thermionic emission, the influence of $R_s$ has been disregarded as it becomes more pronounced at higher bias voltages [37]. However, the $R_s$ values estimated from the plots of $dV/d(\ln I)$–$I$ and $H(I)$–$I$ shown in Fig. 8 are in good accordance with each other, signifying the consistency of the Cheung's functions.

An alternate approach, the Norde function $F(V)$, was used to get more specific information about the diode's $R_s$ and $\Phi_B$ with the following relationships [38]

$$F(V) = \frac{V}{\gamma} - \frac{K_B T}{q} ln\left(\frac{I(V)}{AA^* T^2}\right) \tag{9}$$

where γ is a constant bigger than the diode's ideality factor and $I(V)$ is the current value derived from the $I$–$V$ curve. The minimal point on the $F(V)$–$V$ plots shown in Fig. 9 is used to determine the values of $R_s$ and $\Phi_B$ as follows:

$$\Phi_B = F(V_{min}) + \frac{V_{min}}{\gamma} - \frac{K_B T}{q} \tag{10a}$$

$$R_s = \frac{(\gamma - n)K_B T}{qI_{min}} \tag{10b}$$

The $R_s$ and $\Phi_B$ were found to be 188 and 0.553 for the MS diode, 196 and 0.615 for the MPS1 diode, 192 and 0.740 for the MPS2 SD.

Norde's and Cheung's methods take into account the presence of series resistance, which accounts for the resistance that the current flow through the SD encounters unlike the ideal diode behavior based on TE theory. The accuracy of derived parameters can be affected by the factors such as measurement errors, laboratory conditions in device fabrication, and fitting method restrictions. Norde's method is applied to the full forward bias area of the junction's $I$–$V$ plot, whereas Cheung functions is applied in the region where the $I$–$V$ curve deviates from linearity at high voltage. Therefore, the difference in $R_s$ values obtained from Cheung's method and Norde's method can be attributed to

**Table 2** Comparison of the parameters obtained from Norde and Cheung's methods

| Diode type | $dV/d\ln I$–$I$ | | $H(I)$–$I$ | | Norde | |
|---|---|---|---|---|---|---|
| | $n$ | $R_s$ (Ω) | $R_s$ (Ω) | $\Phi_b$ (eV) | $R_s$ (Ω) | $\Phi_b$ (eV) |
| MS | 7.30 | 140 | 145 | 0.565 | 188 | 0.553 |
| MPS1 | 8.08 | 146 | 175 | 0.581 | 196 | 0.615 |
| MPS2 | 6.92 | 127 | 108 | 0.664 | 192 | 0.740 |

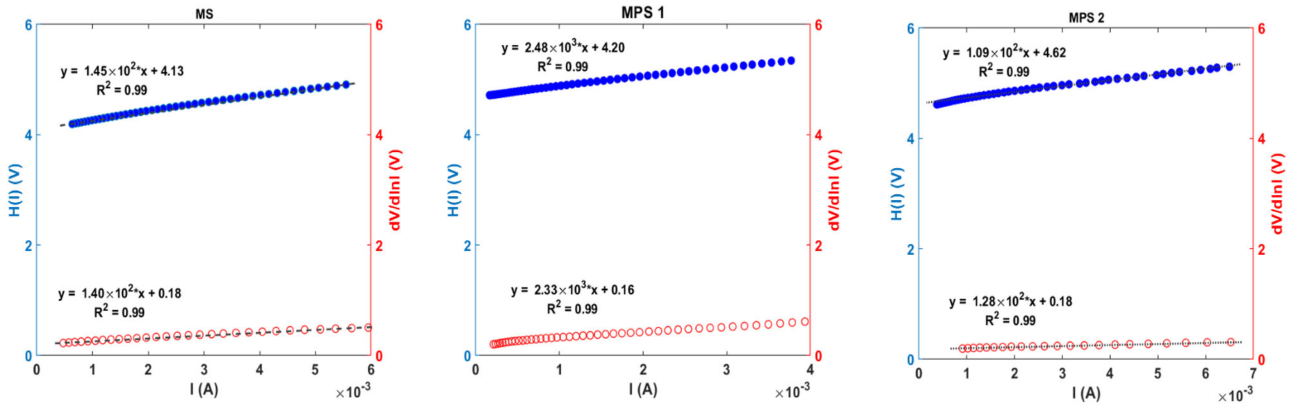



**Fig. 8** *dV/dLn* (*I*) –*I* and *H* (*I*)–*I* plots of MS, MPS1, and MPS2 SDs

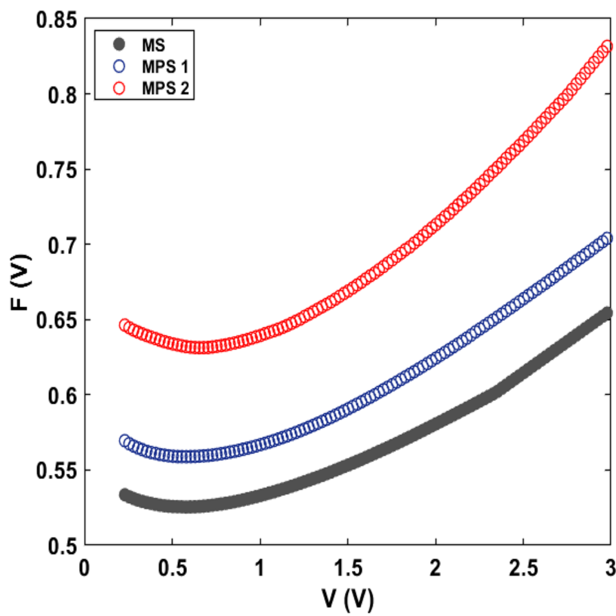



**Fig. 9** The *F* (*V*) –*V* plots of MS, MPS1, and MPS2 SDs

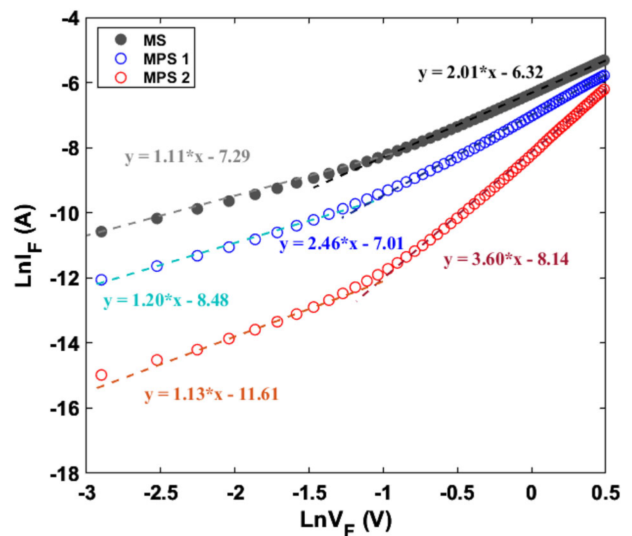



**Fig. 10** The plots of $\mathrm{Ln}I_\mathrm{F}$–$\mathrm{Ln}V_\mathrm{F}$ for MS, MPS1, and MPS2 SDs

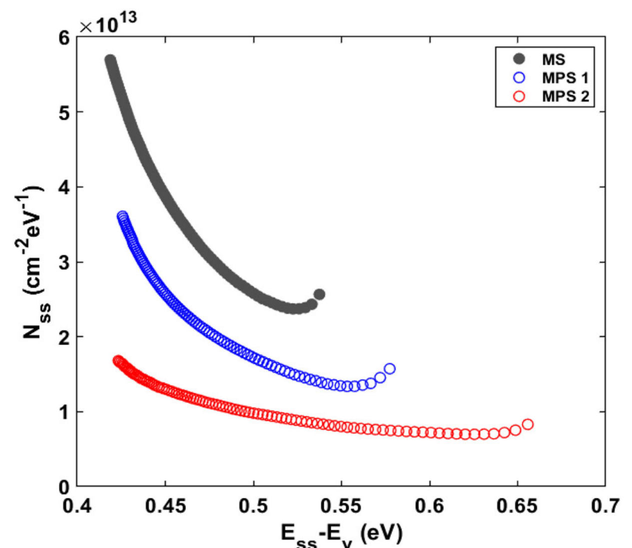



**Fig. 11** Plots of $N_{ss}$ versus $E_{SS}$ –$E_V$ for MS, MPS1, and MPS2 SDs

the different assumptions in each method depending on the non-idealities in the diodes [33–39].

Double logarithmic ln(*I*)–ln(*V*) plots of the MS, MPS1 and MPS2 SDs were also created and shown in Fig. 10, to understand the transport mechanism in detail further. The plots have two unique linear sections with differing slopes due to the current density variations in the form of $I \propto V^m$ [40, 41]. Ohm's law is the predominant mechanism in the first region, with slopes for the three diodes close to unity. The Space Charge Limited Current (SCLC) mechanism is implied by the second region's slopes, which range from 2.01 to 3.60. In this region, the current increases super-linearly, indicating that the distribution of traps is exponential, and m > 2 supports this conclusion [29].

Interface states ($N_{ss}$), referring to electronic states situated close to the interface, can emerge as a result of the

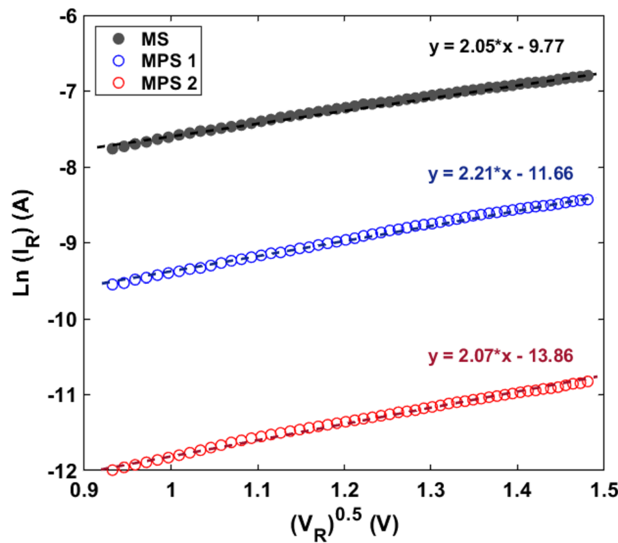



**Fig. 12** Plots of ln ($I_R$)–$(V_R)^{1/2}$ for MS, MPS1, and MPS2 diodes

metal contact-semiconductor or interlayer-semiconductor junction in SBDs Such surface states can have a significant effect on the diode's performance by confining charge carriers and impairing the diode's efficiency. According to Card and Rhoderick [42], the ideality factor n becomes bigger than unity for metal/semiconductor SD with $N_{ss}$ that is in equilibrium with semiconductor and is given by:

$$n(V) = 1 + \frac{d_i}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \tag{11}$$

where $\varepsilon_i$ and $\varepsilon_s$ are the permittivities of the interlayer and the semiconductor, respectively, $\varepsilon_o$ is the permittivity of free space ($=8.85 \times 10^{-14}$ F/cm), $d_i$ is the interlayer thickness $W_D$ is the width of the space charge region. The energy of the $N_{ss}$ relative to the bottom of the conduction band ($E_c$) at the semiconductor's surface can be described in the following formula for n-type semiconductors:

$$E_c - E_{SS} = q(\Phi_e - V) \tag{12}$$

The $N_{ss}$ profiles are shown in Fig. 11, where three diodes exhibit an exponential increase in $N_{ss}$ from the mid-gap toward the top of the $E_v$. The deep-level density of states in the bandgap is the reason for the tails observed in Fig. 10. $N_{ss}$ values range from $5.69 \times 10^{13}$ eV$^{-1}$cm$^{-2}$ at Ec-0.419 eV for the MS SD to $1.68 \times 10^{13}$ eV$^{-1}$cm$^{-2}$ at Ec-0.423 eV for the MPS2 SD. The magnitude of $N_{ss}$ for the MPS2 SD is significantly lower than that of the MS-type SD, indicating that the existence of ZnO/$Ag_2WO_4$–PVP interlayer affects the charge-transport mechanism, diffusion inside the structure and charge interaction type between the metal contact and semiconductor substrate which deactivate the dangling bonds at the surface of the semiconductor substrate.

Additionally, it is clear from Fig.12 that the reverse current of MS, MPS, and MPS2 SDs goes up as the bias increases, but it does not reach saturation. The reverse leakage current mechanism in these structures has been studied by considering the Schottky emission (SE) and Poole-Frenkel emission (PFE) mechanisms across the junction at room temperature. When PFE mechanism is dominant, electrons can pass through the depletion region by means of tunneling. It can happen when the electric field is strong enough to overcome the energy barrier in the depletion region and contributes to the current [43–45]. This contribution is defined by the following equation [40]:

$$I_R = I_{0exp}\left(\frac{\beta_{PFE} V^{1/2}}{K_B T d^{1/2}}\right) \tag{13a}$$

where the $\beta_{PEF}$ is PFE field-lowering coefficient, but when the SE dominates the current, it is

$$I_R = I_{0exp}\left(\frac{\beta_{sc} V^{1/2}}{K_B T d^{1/2}}\right) \tag{13b}$$

where the $\beta_{sc}$ is SE field-lowering coefficient. Theoretical $\beta_{PEF}$ and $\beta_{sc}$ values are provided by

$$\beta_{PFE} = 2\beta_{sc} = \left(\frac{q^3}{\pi\varepsilon_o\varepsilon_r}\right)^{1/2} \tag{14}$$

with relation to the permittivity of the free space ($\varepsilon_o$) and the relative dielectric constant ($\varepsilon_r$). The theoretical values of $\beta_{PEF}$ and $\beta_{sc}$ were calculated as $3.90 \times 10^{-5}$ and $1.95 \times 10^{-5}$ for MS SD, $2.10 \times 10^{-5}$ and $1.05 \times 10^{-5}$ for MPS1 diode, and $1.70 \times 10^{-5}$ and $8.5 \times 10^{-6}$ for MPS2 SD. The experimental values of the field-lowering coefficient were found to be $1.68 \times 10^{-5}$, $3.13 \times 10^{-5}$ and $2.93 \times 10^{-5}$ for MS, MPS1 and MPS2 SDs, respectively, using the slope of the linear region of ln ($I_R$)–$(V_R)^{1/2}$ plots illustrated in Fig. 12. It is clear that the experimental value of field-lowering coefficient for MS diode is close to the corresponding theoretical $\beta_{sc}$ whereas it is close to the corresponding theoretical $\beta_{PEF}$ for MPS1 and MPS2 diodes. This observation suggests that PFE dominates the conduction mechanism in the region of reverse-biased voltage for MPS1 and MPS2 SDs while SE dominates it for MS SD.

## 4 Conclusion

In summary, hydrothermally synthesized ZnO–PVP and ZnO/$Ag_2WO_4$–PVP nanostructures were deposited on

n-Si semiconductor using the spin-coating method. The main electrical parameters and conduction mechanisms of the Au/ZnO–PVP/n-Si (MPS1) and Au/(ZnO/$Ag_2WO_4$–PVP)/n-Si (MPS2) SDs were compared and analyzed to those of the reference MS SD without interfacial layer. The TE, Norde and Cheung's approaches are used to calculate the values of the fundamental device parameters, $n$, $\Phi_B$, and $R_s$. All the SDs exhibit rectifying behavior and in particular, the MPS2 SD has a greater rectification ratio (=332.5) with a lower reverse leakage current when compared to the MS SD. The barrier height obtained from all the abovementioned methods increased with the use of an interfacial layer. The Cheung's method calculates BH values by using data from the nonlinear region of the $I$–$V$ characteristics, which includes the effective contribution of $R_s$, interfacial layer, and interface states. However, because each method uses different regions of the ln$I$–$V$ characteristic, inconsistencies in BH values can occur between the two methods. Similarly, the series resistance values obtained by both methods can also vary due to the same reason. Identifying the position and density of $N_{ss}$ is crucial because low activation energies make it easier for carriers to be released from trap states. It can be concluded from $N_{ss}$ profiles that utilizing an interfacial layer has improved the interface qualities. The SCLC mechanism is dominant as the applied voltage rises, and so does the number of electrons injected into the films from the electrode. Through Schottky or Poole-Frenkel Emission effects, the diode's reverse current transport characteristics were explained. According to calculated average $\beta$ value, the reverse leakage current could be well predicted by the PFE model for MPS1 and MPS2 SDs, suggesting that the primary mechanism for leakage current is the emission of electrons from metal into trap states positioned at the interfacial layer/semiconductor interface.

Concluding, we presented the results by identifying the factors contributing to the non-ideal behavior of the SDs such as $R_s$, $N_{ss}$, high ideality factor, and high leakage current, and proposed strategies to minimize these effects by introducing passivation inorganic and polymer-based composite interlayer. The computed electrical parameters can help in the selection of appropriate materials for SDs with qualities that provide optimal performance for certain applications, such as high-frequency devices, power rectifiers, or photodetectors. Researchers can use these discoveries to improve the performance, efficiency, and reliability of SDs in various applications.

## Compliance with ethical standards

**Conflict of interest** The authors declare no competing interests.

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